IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Patent Application of:

Tony G. Hamilton, et al.

Application No: 09/896,563

Filing Date: June 28, 2001

For: **A METHOD TO PROVIDE DIRECT SYSTEM STORAGE ACCESS WITHIN A NOTEBOOK COMPUTER VIA A WIRELESS INTERCONNECT AND A LOW POWER HIGH-SPEED DATA MANAGEMENT BUS WHILE THE MAIN CPU IS IDLE**

Examiner: Jude Jean Gilles

Art Unit: 2143

Confirmation No.: 7969

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Commissioner for Patents
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

This is an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner of Group 2143, dated August 24, 2006, in which claims 17-40 in the above-identified application were finally rejected. This Appeal Brief is hereby submitted pursuant to 37 C.F.R. § 41.37(a).

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the full interest in the invention, Intel Corporation, 2200 Mission College Blvd. Santa Clara, CA 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the instant appeal.

III. STATUS OF THE CLAIMS

Claims 17-40 are pending in the application and were finally rejected in an Office Action mailed August 24, 2006. Claims 17-40 are the subject of this appeal. A copy of Claims 17-40 as they stand on appeal is set forth in Appendix A.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed August 24, 2006, rejecting claims 17-40, Appellants filed a Notice of Appeal on December 21, 2006. A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 17 claims a method for activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle. (Specification, page 7, lines 11-21; page 4, lines 15-21; Figure 2). Thus, for instance, a notebook in its very deepest sleep state may have its system storage resources used to store or remove data. (Specification, page 4, lines 15-18). The data transfer to the storage device is executed, and system resources are returned to an idle state. (Specification, page 9, lines 9-17; Figure 2).

Independent claim 27 claims a means for activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle. (Specification, page 6, lines 19-21; Figure 1). Claim 27 further claims means for executing

the data transfer to the storage device, and means for returning system resources to an idle state. (Specification, page 6, lines 16-18; Figure 1).

Independent claim 33 claims a machine-readable medium having executable instructions to cause a processor to perform a method for activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle. (Specification, page 7, lines 11-21; page 4, lines 15-21; Figure 2). The data transfer to the storage device is executed, and system resources are returned to an idle state. (Specification, page 9, lines 9-17; Figure 2).

Independent claim 38 claims a computer system that includes a processor coupled to a memory through a bus. (Specification, page 5, line 22 to page 6, line 8; Figure 1). The computer system further includes a unit to activate a storage device in a computer system to transfer data while the processor remains idle. (Specification, page 6, lines 19-21; Figure 1). The unit executes the data transfer to the storage device, and returns system resources to an idle state. (Specification, page 6, lines 16-18; Figure 1).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 17-40 stand rejected under 35 U.S.C. § 103(a) as being obvious under US Patent No. 6,930,987 B1 by Fukuda, et al. (hereinafter "Fukuda") in view of U.S. Patent No. 6,353,927 B1 by Ali, et al. (hereinafter "Ali").

VII. ARGUMENTS

The Claims Are Patentable Over Fukuda In View of Ali

A. Claims 17, 27, 33, 38, and their respective dependent claims 18-26, 28-32, 34-37, and 39-40 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Fukada in view of Ali. Applicant respectfully requests that these rejections be overturned for the following reasons.

In order to establish a *prima facie* case of obviousness: "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." In re Vaech, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, August 2001, §2143.

It is respectfully submitted that a *prima facie* case of obviousness has not been established since: (i) there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings as suggested in the Office Action; and (ii) even when combining the cited references as suggested, the prior art references when combined fail to teach or suggest every claim limitation. Without both these elements, a *prima facie* case of obviousness is not established and a rejection under 35 U.S.C. § 103(a) is improper (MPEP 2143).

(i) THERE IS NO MOTIVATION TO COMBINE REFERENCES

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 FF.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Even if every element of the claimed invention is disclosed by a combination of reference, without a proper motivation to combine, a rejection based on a *prima facie* case of obviousness is improper. *In re Rouffet*, 149 F.3d 1350, 1357 (Fed. Cir. 1998).

In the instant case, it is alleged that the Ali's teachings of a method and apparatus for activating an idle device in a computer system to transfer data while a main processor remains idle would be obvious to combine with the teachings of Fukuda for the purpose of providing a technique to download data into memory in an assembled printed circuit board. Appellant respectfully disagrees.

Fukuda discloses a radio communication CPU 89 that is in a communication idle mode. Upon receiving a control packet from the host CPU, the radio communication CPU shifts from the communication idle mode to an "IN transaction" mode, in which user data from the host CPU can be transmitted to the radio communication CPU. (Fukuda, Col. 20, lines 3-20)

Thus, Fukuda discloses that the host CPU must awaken upon receiving a control packet in order to transfer data. Fukuda teaches away from the claimed invention which allows a main processor to remain in an idle state.

Assuming *arguendo* that Ali teaches activating an idle device in a computer system to transfer data while a main processor remains idle, as asserted in the Office Action, it would not be obvious to combine the teachings of Ali with the teachings of Fukuda. Fukuda requires that the radio communication CPU shift from an idle mode to an IN transaction

mode in order to generate a control packet including user data and transmit the user data. (Fukuda, Col. 20, lines 3-13) The CPU of Fukuda would not be capable of generating or transmitting the user data control packet if it remained in idle mode.

Since Fukuda expressly teaches away from that which is allegedly taught by Ali, Appellant respectfully submits that the skilled artisan would not look to combine Ali with Fukuda. Thus, the rejections of claims 17-40 under 35 U.S.C. § 103(a) are improper. Correspondingly, withdrawal of the obviousness rejection of claims 17-40 is respectfully requested and allowance of such claims is requested.

(ii) NEITHER FUKUDA NOR ALI DISCLOSES, TEACHES OR SUGGESTS APPELLANT'S CLAIMED ELEMENT

Independent claims 17, 27 and 33 each recite the limitation of "activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle." Independent claim 38 recites "activate a storage device in a computer system to transfer data while the processor remains idle."

Fukuda does not disclose "activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle." In contrast, Fukuda requires that the radio communication CPU shift from an idle mode to an IN transaction mode in order to generate a control packet including user data and transmit the user data. (Fukuda, Col. 20, lines 3-13) Thus, Fukuda does not disclose "activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle." The Office Action implies this deficiency in Fukuda at the bottom of page 3 and the top of page 4, when providing the rationale for the combination of Ali with Fukuda.

Ali does not disclose "activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle." Ali discloses the use of an external processor to hold an on-board processor in a reset state so that control signals may be accessed by the external processor. Upon determining a suitable time, perhaps when the on-board processor has entered an idle or otherwise suitable state, the external processor takes control of control signals by activating a reset signal to the on-board processor, which causes the on-board processor to relinquish control of the control signals. The on-board processor is held in a reset condition until the external processor completes its tasks. (Ali, Abstract; Col. 3, lines 18-26, Col. 4, lines 36-49) Thus, the on-board processor of Ali enters an idle state, but does not remain in the idle state. The on-board processor of Ali is forced into a reset condition from the idle state, and remains in the reset condition.

Thus, Ali also teaches away from the claimed invention, which allows a main processor to remain in an idle state. The processor of Ali does not remain in an idle state. Instead, an external processor detects when the on-board processor is idle (and thus not utilizing the control signals), and subsequently forces the on-board processor into a reset state so that the external processor can operate the control signals. Therefore, Ali does not disclose "activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle."

Because Fukuda and Ali, either individually or in combination, do not teach or suggest each and every limitation of independent claims 17, 27, 33 and 38, withdrawal of the obviousness rejection of claims 17, 27, 33 and 38 and their associated dependent claims is respectfully requested.

VIII. CONCLUSION

Appellant submits that no motivation exists to combine Fukuda with Ali to achieve the elements of Appellant's invention. Appellant submits that the 35 U. S. C. § 103 (a) rejection of the claims is further improper because neither Fukuda nor Ali discloses, teaches, or suggests Appellant's claimed element.

Appellant respectfully submits that in view of the foregoing, all pending claims in this application are patentable over the cited prior art reference, alone, or in any combination. Appellant respectfully requests that the Board of Patent Appeals and Interferences overturn the Examiner and direct allowance of the rejected claims.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 50-0221 for any charges that may be due. Furthermore, if an extension is required, then Appellant hereby requests such extension.

Respectfully submitted,

Dated: March 20, 2007

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A. Appendix of claims

1-16 (Cancelled)

17. (Previously Presented) A method, comprising:
activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle;
executing the data transfer to the storage device; and
returning system resources to an idle state.

18. (Previously Presented) The method of claim 17, further comprising:
buffering the data for transfer.

19. (Previously Presented) The method of claim 17, further comprising:
detecting a request for data transfer to activate the idle storage device while the main processor of the computer system is idle.

20. (Previously Presented) The method of claim 19, wherein a controller activates the idle storage device by directing power to the device.

21. (Previously Presented) The method of claim 17, further comprising:
tagging the transferred data for recognition.

22. (Previously Presented) The method of claim 17, further comprising:
apportioning a system time and power resource based on the transferred data.

23. (Previously Presented) The method of claim 22, further comprising:
returning the system resource to a pre-transfer state.

24. (Previously Presented) The method of claim 17, further comprising:

notifying a user of the computer system of the data transfer after the system is returned to an idle state.

25. (Previously Presented) The method of claim 17, wherein the data is transferred wirelessly.

26. (Previously Presented) The method of claim 17, wherein the data is transferred via a low level data bus.

27. (Previously Presented) An apparatus comprising:

means for activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle;

means for executing the data transfer to the storage device; and

means for returning system resources to an idle state.

28. (Previously Presented) The apparatus of claim 27, further comprising:

means for buffering the data for transfer.

29. (Previously Presented) The apparatus of claim 27, wherein the means for activating the idle storage device comprise a controller that detects a request for data transfer while the main processor of the computer system is idle.

30. (Previously Presented) The apparatus of claim 29, wherein the controller activates the idle storage device by directing power to the device.

31. (Previously Presented) The apparatus of claim 27, wherein the data is transferred wirelessly.

32. (Previously Presented) The apparatus of claim 27, wherein the data is transferred via a low level data bus.

33. (Previously Presented) A machine-readable medium having executable instructions to cause a processor to perform a method, the method comprising:

activating an idle storage device in a computer system to transfer data while a main processor of the computer system remains idle;

executing the data transfer to the storage device; and

returning system resources to an idle state.

34. (Previously Presented) The machine-readable medium of claim 33, wherein the method further comprises:

buffering the data for transfer.

35. (Previously Presented) The machine-readable medium of claim 34, wherein the idle storage device is activated by a controller that detects a request for data transfer while the main processor of the computer system is idle.

36. (Previously Presented) The machine-readable medium of claim 33, wherein the method further comprises:

apportioning a system resource based on the transferred data.

37. (Previously Presented) The machine-readable medium of claim 36, wherein the method further comprises:

returning the system resource to a pre-transfer state.

38. (Previously Presented) A computer system comprising:

a processor coupled to a memory through a bus;

a unit to activate a storage device in a computer system to transfer data while the processor remains idle, the unit to

execute the data transfer to the storage device, and the unit to

return system resources to an idle state.

39. (Previously Presented) The system of claim 38, further including a buffer to store data to be transferred.

40. (Previously Presented) The system of claim 38, further including a unit to detect a request for data transfer to activate the idle storage device while the main processor of the computer system is idle.

B. Evidence Appendix

No additional evidence is being submitted with this appeal brief.

C. Proceeding Appendix

No other related proceedings exist at this time.